

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

- 1 1. (Currently Amended) An inductor in an integrated circuit, comprising:
2 a conductive trace disposed over an insulating layer, said insulating layer overlying a
3 semiconductor substrate of a first conductivity type; and
4 at least two deep wells of opposite conductivity type in said substrate underneath said
5 [[track]] trace, wherein said deep wells are continuous for at least 1.5 μ m approximately from a
6 surface of said substrate underneath said insulating layer.
- 1 2. (Original) The inductor of claim 1 wherein said conductive trace comprises metal.
- 1 3. (Original) The inductor of claim 1 wherein said semiconductor substrate is a p-type
2 substrate and said deep wells are n-type wells
- 1 4. (Original) The inductor of claim 1 wherein said semiconductor substrate is an n-type
2 substrate and said deep wells are p-type wells.
- 1 5. (Original) The inductor of claim 1 wherein said deep wells are not reverse biased.
- 1 6. (Original) The inductor of claim 1 wherein said deep wells are arranged in a pattern to
2 form a substantial depletion space in said substrate underneath said trace.
- 1 7. (Original) The inductor of claim 1 wherein said deep wells are cuboid.
- 1 8. (Original) The inductor of claim 1 wherein said deep wells are L shaped cuboid.
- 1 9. (Canceled)
- 1 10. (Canceled)

- 1 11. (Original) The inductor of claim 1 wherein said deep wells are formed by ion
2 implantation.
- 1 12. (Original) The inductor of claim 11 wherein said ion implantation comprises a first stage
2 in which ions are accelerated to a first energy level and at least a second stage in which ions are
3 accelerated to an energy level different from said first energy level.
- 1 13. (Original) An inductor in an integrated circuit, comprising:
2 a conductive trace disposed over an insulating layer, said insulating layer overlying a
3 semiconductor substrate of a first conductivity type;
4 a shallow trench isolation region, formed in said substrate underneath said trace; and
5 at least two deep wells of opposite conductivity type in said substrate underneath said
6 shallow trench isolation region.
- 1 14. (Original) The inductor of claim 13 wherein said conductive trace comprises metal.
- 1 15. (Original) The inductor of claim 13 wherein said shallow trench isolation comprises
2 silicon dioxide.
- 1 16. (Original) The inductor of claim 13 wherein said semiconductor substrate is a p-type
2 substrate and said deep wells are n-type wells.
- 1 17. (Original) The inductor of claim 13 wherein said semiconductor substrate is an n-type
2 substrate and said deep wells are p-type wells.
- 1 18. (Original) The inductor of claim 13 wherein said deep wells are not reverse biased.
- 1 19. (Original) The inductor of claim 13 wherein said deep wells are arranged in a pattern to
2 form a substantial depletion space in said substrate underneath said trace.
- 1 20. (Original) The inductor of claim 13 wherein said deep wells are cuboid.

- 1 21. (Original) The inductor of claim 13 wherein said deep wells are L shaped cuboid.
- 1 22. (Original) The inductor of claim 13 wherein said deep wells are continuous.
- 1 23. (Original) The inductor of claim 22 wherein said deep wells are continuous for at least
2 1.5 μm approximately from a plane in said substrate underneath and adjacent to said shallow
3 trench isolation region.
- 1 24. (Original) The inductor of claim 13 wherein said deep wells are formed by ion
2 implantation.
- 1 25. (Original) The inductor of claim 24 wherein said ion implantation comprises a first stage
2 in which ions are accelerated to a first energy level and at least a second stage in which ions
3 are accelerated to an energy level different from said first energy level.
- 1 26. (Canceled)
- 1 27. (Canceled)
- 1 28. (Canceled)
- 1 29. (Canceled)
- 1 30. (Canceled)
- 1 31. (Canceled)
- 1 32. (Canceled)
- 1 33. (Canceled)

1 34. (Canceled)

1 35. (Canceled)

1 36. (Canceled)

1 37. (Canceled)

1 38. (Canceled)

1 39. (Canceled)

1 40. (Canceled)

1 41. (Canceled)

1 42. (New) An inductor in an integrated circuit, comprising:
2 a conductive trace disposed over an insulating layer, said insulating layer overlying a
3 semiconductor substrate of a first conductivity type; and
4 at least two deep wells of opposite conductivity type in said substrate underneath said
5 trace, wherein said deep wells are not reverse biased.